# PROCESS AND DEVICE FOR DETERMINISTIC TRANSMISSION OF ASYNCHRONOUS DATA IN PACKETS



## DESCRIPTION

### Technical field

The present invention relates to a process and device for deterministic transmission of asynchronous data in packets.

### Status of the previous technique

In devices of the prior art for deterministic transmission of asynchronous data in packets, the acquisition device and data acquired by this device are asynchronous. Data packeting is conducted according to an inherent sequencing. A packet corresponds to one or several acquired data processed with or without wrapping, the wrapping being made up of a heading and an end. The number of data transmitted in the output message corresponding to a packet is defined according to two criteria:

the number of data is restricted:

- it is always the same, or
- the maximum is specified

the distribution of data may or may not be positioned temporally in an equally-timed manner.

In the first example of data transmission from a packet i in the output message, as illustrated in figure 1, the number of data Mi is always the same, and distributed in an equally-timed manner (Ti equal delays).

In the second example of data transmission from a packet i in the output message, as illustrated in figure 2, the maximum number of data Mi is always the same, it is MxTxi over an identified period of time Txi, and distributed in an unequally-timed manner (Txi variable delays) – that is, MxTxi varies at each Txi, with $MxTxi \leq Mi$.

In the field of data acquisition and telemetry of flight testing installations, the numerical or digital data, conveyed on continuous and cyclic messages, issued by acquisition and processing systems of the prior art is stored in the FIFO (First in - First out) registers as and when it arrives. The data arrives in a totally asynchronous manner.

A module for packeting facilitates placing certain data from these FIFO registers according to a predefined order. It also facilitates enhancing this data with elements of the relative date calculation type, data identification, and formatting of data, etc. A packet thus obtained is therefore a group of data with a precise format and containing data in a precise order.

A module for packeting operates according to the following succession of stages:

1) reception of data contained in the FIFO registers (dump),

2) start of packeting,

3) packeting, with sorting and data enhancement,

4) end of packeting,

5) sending of the assembled packet to a message composition module.

The message composition module recovers, one after the other, the assembled packets created by the packeting modules. A message is then composed using successive assembled packets in a predefined order.

A formatting module then facilitates setting the message into the proper protocol used for transmission.

The operating cycle of the packeting module is self-sustaining. When the message composition module needs a packet, it sends a request to the packeting module which transmits the packet if it is made up, i.e. if stage 4 is finished. If not, it sends nothing or else an empty packet so as not to block the message composition module. The data is transmitted via the various stages 1 to 5 - the data arrives, it is assembled into packets by a self-sustaining device which has its own life cycle, as it is only transferred in the message if the packet is ready. It is even possible that the message can contain no data, simply because the packeting has not been finished.

In these devices of the prior art, the data conveyed on the messages is at fixed slots in time. They are PCM (Pulse Coded Modulation) type messages which meet the IRIG106 standard. The formalism of packeting, as a packet can be made up of one datum, is standardized. On the other hand, this standard stipulates nothing on the transmission time of the packets. It is the same for the CE83 and CCSDS standards.

As illustrated in figure 3, the data and transmission in the output message are asynchronous, the transmission time TT therefore varies between the time of packeting TP and a duration 2*TP equal to twice this time, as the transmission time in the output message TMS is such that TMS<<TP.

One object of the invention is to mitigate the disadvantages of devices of the prior art, by enabling:

- transmission of the maximum amount of data in the output message,
- controlling transmission time of the acquired data,
- realizing the greatest possible ratio for the number of acquired/wrapped data in the packet.

**Summary of the invention**

The invention relates to a process of deterministic transmission of asynchronous data in packets, in which data arriving asynchonously is stored in registers as and when it arrives, the said process, for example, comprising the following stages:

- reception of data contained in a set of registers in one of several packeting modules; start of packeting or packet assembly; packeting with sorting and enhancement of data; end of packeting; and sending of the packet assembled in this matter,
- terminating packet assembly in the course of realization in a packeting module when a message composition module needs the packet; transmission of the packet assembled; and start of the realization cycle of a new packet,

- recovery, one after another, of packets thus created in a predefined order in the message composition module,

- setting the message, compiled in the message composition module, in the proper protocol used for transmission.

In accordance with this process, a packeting module which is no longer self-sustained therefore is used. As soon as the message composition module requests a packet, it receives the packet since it is this composition module that controls the packeting cycle.

In contrast to devices of the prior art in which the messages are only compiled with "well finished" packets (with the risk of having empty packets), in the process of the invention each message may carry packets perhaps "less well finished," but all the data which can be, is transmitted as soon as transmission is requested. The timing cycle of datum between input and output of a device implementing this inventive process is therefore controlled.

The invention also relates to a device of deterministic transmission of asynchronous data in packets comprising:

- at the least one input module receiving the input data,

- registers receiving numerical data stemming from this input module,

- several packeting modules each connected to at least one register,

- at least one control module for register dump monitored by at least one packeting module,

- a message composition module receiving the outputs of all the packeting modules, which can send an order of end of packet assembly to each packeting module,

- a module for formatting packets,

- an output module capable of issuing each made-up packet on a transmission line.

The process and the device of the invention can be used notably in data acquisition and real-time processing systems for test installations for new airplanes. The solution proposed in the invention for such systems offers the following advantages. To follow vibration (or flutter) tests which are very dangerous for a plane, it is essential to perfectly control the

transmission time TT, as the useful acquired data must be given to a specialist with a delay TT either less than 100ms, or parameterized depending on the type of test. With the solution stipulated in the invention TT = TP, while in the devices of prior art TP<TT<_2*TP on the assumption that TMS<<TP. The objectives are therefore optimized with the solution of the invention. In fact, at fixed TT, TP is greater with the recommended solution than with the solution of devices of the prior art.

**Short description of the drawings**

- Figures 1 and 2 illustrate two examples of transmission of data from a packet, in a device of the prior art.

- Figure 3 illustrates an example of operation of a device of the prior art.

- Figure 4 illustrates the operation of a process in accordance with the invention.

- Figure 5 illustrates a device in accordance with the invention.

- Figure 6 illustrates an example of operation of a device in accordance with the invention illustrated in figure 5.

- Figures 7 and 8 illustrate an example of realization for an acquisition of arinc429 bus using respectively a device of the prior art and the device in accordance with the invention.

**Summary of realization methods**

A process of deterministic transmission of asynchronous data in packets in accordance with the invention in which data arriving asynchronously is stored in FIFO registers as and when it arrives, includes the following stages:

- reception of data contained in the registers,
- start of packeting or packet assembly,
- packeting with sorting and enhancement of data,
- end of packeting,

- sending of the packet to a message composition module which recovers the packets created one after another, in a predefined order,

and, when this message composition module needs a packet:

- terminating packet assembly in the course of realization,
- transmission of the packet thus assembled,
- start of the realization cycle of a new packet.

As illustrated in figure 4, the process of the invention consists in synchronizing the start and end of packet make-up, or assembly, in relation to their transmission in the output message - TMS being the transmission time in the output message, TP the packeting time and TT the transmission time with TT = TP + TMS. The solution obtained with TP>>TMS advantageously meets the above-specified objectives.

For an identified packet, the packeting limits the number of acquired data to a value x. If during the time TP, there are x + m data to be packeted, m data is then lost.

The device of the invention, illustrated in figure 5, comprises:

- at least one input module 10 receiving input data, for example a digital bus BN and analog data DA,

- at least a set of registers 11 receiving digital data from the input module, possibly through an analog/digital converter 12, connected to at least one packeting module 13,

- at the least one control module for register dump 14 monitored by at least one packeting module 13,

- a message composition module 15 receiving the outputs of all the packeting modules 13, which can send an order of end of packet make-up or assembly to each one of the packeting modules,

- a module for formatting packets 16,

- an output module 17 capable of issuing each made-up packet on a transmission line 18.

In the device of the invention, the digital or digitized data is stored in the FIFO registers 11 as and when it arrives. The data arrives in a totally asynchronous manner, and seen from the device, its arrival is random.

The role of each packeting module 13 is to place certain data from the registers 11 according to a predefined order. It can also enhance this data with elements of the relative date calculation type, data identification and formatting of the data. A packet is therefore a group of data with a precise format and containing data in a precise order.

As described previously, each packeting module 13 operates according to the following cycle:

1) reception of the data contained in the registers,

2) start of the packeting,

3) packeting with sorting and enhancement of the data,

4) end of the packeting,

5) sending of the packet to the message composition module.

One difference between the device of the invention and devices of the prior art is the way in which each task 1 to 5 is triggered.

The message composition module 15 recovers the packets created by the successive packeting modules 13 one after the other in a predefined order.

The operating cycle of the module 13 is not self-sustaining. When the message composition module 15 needs a packet, it sends the packet request to the packeting module 13. This stops makeup or assembly of the packet in the course of realization. The packeting module 13 transmits the packet thus made up or assembled, then starts the realization cycle of a new packet.

The formatting module 16 is responsible for setting the message 15 in electrical format in the protocol used for the transmission (recognized function and realization).

In an example of operation, the device of the invention comprises three packeting modules 13. The make-up of packets that they generate (P1, P2 and P3 respectively) is

unimportant (data sorting, enhancing, etc.). As illustrated in figure 6, a message is made up of the succession of three packets - P1 followed by P2 followed by P3 - which are transmitted by the message composition module 15 to the formatting module 16, TP being the packeting time. In this example wrapping elements are not taken into consideration (start of frame, end of frame, checksum, etc.) realized by the formatting module 16.

At present an example of realization will be considered which is an acquisition of arinc429 bus on the assumption that TMS<<TP, TCB being the bus cycle time, the number of data always being the same, and distributed in an equally-timed manner:

- figure 7 illustrates operation of a device of the prior art,
- figure 8 illustrates operation of the device of the invention as described above.

Advantages of the solution proposed by the invention as compared with devices of the prior art are shown in Table 1 at the end of the description. The device of the invention meets the objectives defined previously and reveals a very significant gain as compared with the devices of the prior art.

**Table 1**

| Output message for the time window TT | Device of the prior art | Device of the invention | Device of the prior art – Device of the invention/Device of the invention => gain |
|---|---|---|---|
| Number of data | 18 | 11 | 64% |
| Number of wrappings | 2 | 1 | 100% |